2nd Workshop on Open-Soure Design Automation
OSDA 2020

Field-programmable gate array (FPGA) technology is becoming more and more relevant: recent examples include Intel's acquisition of Altera in 2015, Amazon's 2016 announcement of FPGAs within their AWS cloud infrastructure, and Microsoft's statement in 2018 that more than 100K FPGAs were deployed in their Azure cloud for machine learning acceleration. With traditional cloud infrastructure -- which are mainly processor based -- software engineers have a choice of open-source (e.g. GNU GCC, Clang) and proprietary compilers (Microsoft, Intel) to use. However, the wide availability of FPGA technology contrasts with the narrow ways in which one can access them -- through proprietary tools.

There is no doubt that proprietary EDA tools are successful, mature, and are fundamental for hardware development. However, the "walled garden" approach created by closed-source toolflows can hamper novel FPGA-based applications and EDA innovation alike by requiring that researchers either operate within the limits of what has already been imagined, or require that they attempt to simulate their effects on incomplete models, potentially leading to incorrect conclusions. For such an off-the-shelf field-programmable technology, unlike fixed-function ASICs, this seems like a lost opportunity.

Another recent development has been growing activity in the open-source community to produce open equivalents of EDA tools, as well as efforts to document FPGA architectures. For instance, Yosys has been widely used for behavioral synthesis since 2012 and Project Icestorm, the first fully open-source FPGA design flow has been available since 2015; together they enabled Trenz Electronic's icoBOARD, a Raspberry Pi accessory that could be programmed entirely using its ARM CPU, a platform not otherwise supported by the vendor. The availability of low-cost FPGA development boards such as the icoBOARD, TinyFPGA, IceZUM Alhambra, amongst others have also played a part in fostering this "Open FPGA" movement. The advantages of open design automation -- as Linux has provided for operating systems -- are many: unrestricted research and development, improved quality due to competition, teaching benefits, as well as lowering the barrier and risk to entry, and time to market, of start-ups for building novel FPGA applications, tools, and silicon. With such an open-source ecosystem in place, reprogrammable logic could achieve the same success and inspire the next generation of hardware engineers as the Raspberry Pi has done for software engineers.

This workshop intends to provide an avenue for industry, academics, and hobbyists to collaborate, network, and share their latest visions and open-source contributions, with a view to promoting reproducibility and reusability in the design automation space. DATE provides the ideal venue to reach this audience since it is the flagship European conference in this field -- particularly poignant due to the recent efforts across the European Union (and beyond) that mandate "open access" for publicly funded research to both published manuscripts as well as software code necessary for reproducing its conclusions. A secondary objective of this workshop is to provide a peer-reviewed forum for researchers to publish "enabling" technology such as infrastructure or tooling as open-source contributions -- standalone technology that would not normally be regarded as novel by traditional conferences -- such that others inside and outside of academia may build upon it.

Topics of interest

- Open-source FPGA tools -- the latest developments, breakthroughs, challenges and surveys on the toolflows required to target real silicon parts: synthesis, simulation, place and route, etc.
- Open-source IP for FPGAs -- contributions that enrich the IP ecosystem and reduce the need to "re-invent the wheel", e.g. PCIe and DDR controllers, debug infrastructure, etc.
- Design methodologies provided as open-source -- such as hardware description languages (e.g. MyHDL, Chisel), domain specific (DSL), high level synthesis (HLS), or asynchronous methods.
- Directions on where the open-source FPGA movement should go, current weaknesses in the toolchain, and/or perspectives from industry on how open-source can affect aspects of safety, security, verification, IP protection, time-to-market, datacenter/cloud infrastructure, etc.
- Discussions and case studies on how to license, acquire funding, and commercialise technologies surrounding open-source hardware, which may be different to open software.

Important dates:

Submission deadline:	January 12, 2020
Acceptance notification:	January 19, 2020
Camera-ready final version:	February 19, 2020
Workshop:	March 13, 2020

Submission details and requirements:

Prospective authors are invited to submit original contributions (up to six pages), extended abstracts describing work-in-progress or position papers (not exceeding two pages), and demo proposals that would be of general interest. Papers must be submitted as an A4-sized PDF, in the IEEE conference format.

In line with OSDA's mission, we encourage and will favour submissions that make all artifacts used for experimentation (benchmarks, code, etc.) available for private peer-review. Accepted submissions are required to publish these artifacts under an OSI-approved (preferably permissive) license.

The proceedings of this workshop containing all accepted papers will be published on the open-access arXiv repository. Every accepted paper must have at least one author registered to attend the workshop by 31 January. Selected papers may also be considered for a special-issue journal.

Submission link: https://easychair.org/conferences/?conf=osda2020

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- Andrea Borga, oliscience, Netherlands
- Xin Fang, Qualcomm, USA
- Hipolito Guzman-Miranda, University of Seville, Spain
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- Davide Rossi, University of Bologna, Italy

Organizing team

Clifford Wolf, SymbioticEDA, Austria

Christian Krieg, TU Wien, Austria